Amendments to the Specification:

Please amend the paragraph beginning on page 2, line 3 as follows:

This is a related application to a co-pending U.S. Patent application entitled "DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE", having serial number ~~10/459,979~~10/459,797, filed June 12, 2003, having Leather et al. as the inventors, owned by the same assignee and hereby incorporated by reference in its entirety.

Please amend the paragraph beginning on page 11, line 16 as follows:

In operation, graphics assembly unit 510 takes transformed vertices data and assembles complete graphics primitives – triangles or parallelograms, for instance. A set-up unit 515 receives the data output from graphics assembly 510 and generates slope and initial value information for each of the texture address, color, or Z parameters associated with the primitive. The resulting set-up information is passed to 2 or more identical pipelines. In the current example there are two pipelines, pipeline 520 and pipeline 525, but the present invention contemplates any configuration of parallel pipelines. In this example, each pipeline 520 and 525 owns one-half of the screens pixels. Allocation of work between the pipelines is made based on a repeating square pixel, tile pattern. In one embodiment, logic 530 in the set-up unit 515 intersects the graphics primitives with the repeating tile pattern such that a primitive is only sent to a pipeline if it is likely that it will result in the generation of covered pixels. The functionality of a setup unit is further described in commonly owned co-pending U.S. Patent Application entitled "Scalable Rasterizer Interpolator", with serial number ~~10/xxx,xxx,~~10/730,864, filed December [[XX]]8, 2003, and is hereby fully incorporated by reference.

Please amend the paragraph beginning on page 13, line 5 as follows:

Each pipeline contains an input FIFO 535 used to balance the load over different pipelines. A scan converter 540 works in conjunction with Hierarchical Z interface of Z buffer logic 555 to step through the geometry (e.g., triangle or parallelogram) within the bounds of the pipeline's tile pattern. In one embodiment, initial stepping is performed at a coarse level. For each of the coarse level tiles, a minimum (i.e., closest) Z value is computed. This is compared with the farthest Z value for the tile stored in a hierarchical Z buffer 550. If the compare fails, the tile is rejected. The functionality of the scan converter and Hierarchical Z interface is further described in commonly owned co-pending U.S. Patent Application entitled "Scalable Rasterizer Interpolator", with serial number ~~10/xxx,xxx,~~10/730,864, filed December [[XX]]8, 2003, and is hereby fully incorporated by reference.

Please amend the paragraph beginning on page 13, line 15 as follows:

The second section of the scan converter 540 works in conjunction with the Early Z interface of the Z buffer logic 550 to step through the coarse tile at a fine level. In one embodiment, the coarse tile is subdivided into 2x2 regions (called "quads"). For each quad, coverage and Z (depth) information is computed. A single bit mode register specifies where Z buffering takes place. If the current Z buffering mode is set to "early", each quad is passed to the Z buffer 555 where its Z values are compared against the values stored in the Z buffer at that location. Z values for those covered pixels which "pass" the z compare, are written back into the Z buffer, and a modified coverage mask describing the result of the Z compare test is passed back to the scan converter 540. At this stage, those quads for which none of the covered pixels passed the Z compare test are discarded. The early Z functionality attempts to minimize the

amount of work applied by the unified shader and texture unit to quads which are not visible. The functionality of the scan converter and Early Z interface is further described in commonly owned co-pending U.S. Patent Application entitled "Scalable Rasterizer Interpolator", with serial number ~~10/xxx,xxx,~~10/730,864, filed December [[XX]]8, 2003, and is hereby fully incorporated by reference.

Please amend the paragraph beginning on page 14, line 19 as follows:

The functionality of a unified shader is further described in commonly owned co-pending U.S. Patent Application entitled "Unified Shader", with serial number ~~10/xxx,xxx,~~10/730,965, filed December [[XX]]8, 2003, and is hereby fully incorporated by reference.